## AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Please amend claims 1, 3, 4, 7 – 11, 14, 17 – 23, 25 – 32, 35, 41, 45, 63, 66, 71, 75, and 89 – 100, cancel claim 6, and add new claims 101 – 143, as follows:

1 (Currently Amended). A system for adaptive configuration, the system comprising:

a memory adapted to store a first set of configuration information, the first set of configuration information comprising a first subset of configuration information and a second subset of configuration information;

a first plurality of ~~heterogeneous~~ fixed and differing computational elements; ~~elements, a first computational element of the plurality of heterogeneous computational elements having a first fixed architecture and a second computational element of the plurality of heterogeneous computational elements having a second fixed architecture, the first fixed architecture being different than the second fixed architecture; and~~

a second plurality of fixed and differing computational elements; and

an interconnection network coupled to the ~~plurality~~ first and second pluralities of computational elements and to the memory, the interconnection network comprising a plurality of switching elements and a plurality of routing elements, ~~of heterogeneous computational elements~~, the interconnection network adapted to configure ~~capable of configuring~~ the first plurality of ~~heterogeneous~~ computational elements for a first functional mode of a plurality of functional modes in response to the first subset of configuration information, and the interconnection network further adapted to configure ~~capable of reconfiguring~~ the second plurality of ~~heterogeneous~~ computational elements for a second, different functional mode of the plurality of functional modes, in response to the second subset of configuration information, ~~information, the first functional mode being different than the second functional mode.~~

2 (Original). The system of claim 1, wherein the first set of configuration information provides a first system operating mode.

3 (Currently Amended). The system of claim 2, ~~further comprising:~~ wherein the memory is further adapted to store a second set of configuration information, the second set of configuration information providing a second system operating mode.

4 (Currently Amended). The system of claim 3, wherein the first set of configuration information corresponds to a first system ~~reconfiguration~~ configuration capacity and the second set of configuration information corresponds to a second system ~~reconfiguration~~ configuration capacity.

5 (Original). The system of claim 1, wherein the first set of configuration information is selected from a plurality of sets of configuration information.

6 (Cancelled).

7 (Currently Amended). The system of claim 1, wherein the ~~first set of configuration information is stored in~~ memory comprises a second plurality of ~~heterogeneous~~ computational elements configured for a memory functional mode.

8 (Currently Amended). The system of claim 1, wherein the memory comprises ~~first set of configuration information is stored as~~ a configuration of the plurality of ~~heterogeneous~~ computational elements in response to the first set of configuration information.

9 (Currently Amended). The system of claim 1, wherein the first set of configuration information is transferred to the system from ~~stored in~~ a machine-readable medium.

10 (Currently Amended). The system of claim 1, wherein the first set of configuration information is transmitted to the system through a wireless ~~an air~~ interface.

11 (Currently Amended). The system of claim 1, wherein the first set of configuration information is transmitted to the system through a wireline interface.

12 (Original). The system of claim 1, wherein the first set of configuration information is embodied as a plurality of discrete information data packets.

13 (Original). The system of claim 1, wherein the first set of configuration information is embodied as a stream of information data bits.

14 (Currently Amended). The system of claim 1, wherein the first fixed architecture and the second fixed architecture are selected from a plurality of ~~specific~~ fixed architectures, the plurality of ~~specific~~ fixed architectures comprising a fixed architectures adapted to perform at least two of the following corresponding functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability.

15 (Previously Presented). The system of claim 1, wherein the plurality of functional modes comprises at least two of the following functional modes: linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.

16 (Original). The system of claim 1, wherein the first subset of configuration information and the second subset of configuration information are commingled with data to form a singular bit stream.

17 (Currently Amended). The system of claim 1, further comprising:

a controller coupled to the plurality of ~~heterogeneous~~ computational elements and to the interconnection network, the controller adapted to direct and schedule ~~capable of directing and scheduling~~ the configuration of the first plurality of ~~heterogeneous~~ computational elements for the first functional mode and the ~~reconfiguration~~ configuration of the second plurality of ~~heterogeneous~~ computational elements for the second functional mode.

18 (Currently Amended). The system of claim 17, wherein the controller is further ~~capable of timing and scheduling~~ adapted to time and schedule the configuration of the first and second pluralities of ~~and reconfiguration of the plurality of heterogeneous~~ computational elements with corresponding data.

19 (Currently Amended). The system of claim 17, wherein the controller is further adapted to select ~~capable of selecting~~ the first subset of configuration information and the second subset of configuration information from a singular bit stream containing data commingled with the first set of configuration information.

20 (Currently Amended). The system of claim 1, ~~further comprising:~~

~~a second plurality of heterogeneous computational elements coupled to the interconnection network,~~ wherein when the second plurality of ~~heterogeneous~~ computational elements are configured for a controller operating mode, the second plurality of ~~heterogeneous~~ computational elements adapted to direct and schedule ~~capable of directing and scheduling~~ the configuration of the first plurality of ~~heterogeneous~~ computational elements for the first functional mode. ~~mode and the reconfiguration of the plurality of heterogeneous computational elements for the second functional mode.~~

21 (Currently Amended). The system of claim 20, wherein the second plurality of ~~heterogeneous~~ computational elements is further adapted to time and schedule ~~capable of timing and scheduling~~ the configuration ~~and reconfiguration~~ of the first plurality of ~~heterogeneous~~ computational elements with corresponding data.

22 (Currently Amended). The system of claim 20, wherein the second plurality of ~~heterogeneous~~ computational elements is further adapted to select ~~capable of selecting~~ the first subset of configuration information and the second subset of configuration information from a singular bit stream containing data commingled with the first set of configuration information.

23 (Currently Amended). The system of claim 1, wherein the system is embodied within a mobile station having a plurality of operating modes.

24 (Previously Presented). The system of claim 23, wherein the plurality of operating modes of the mobile station comprises at least two of the following modes: a mobile telecommunication mode, a personal digital assistance mode, a multimedia reception mode, a mobile packet-based communication mode, and a paging mode.

25 (Currently Amended). The system of claim 1, wherein the system is embodied within a server having a plurality of operating modes.

26 (Currently Amended). The system of claim 1, wherein the system is embodied within an adjunct network entity having a plurality of operating modes.

27 (Currently Amended). The system of claim 1, wherein the first plurality of ~~heterogeneous~~ computational elements are configured to generate a request for a second set of configuration information for ~~, the second set of configuration information providing~~ a second system operating mode.

28 (Currently Amended). The system of claim 27, wherein the first plurality of ~~heterogeneous~~ computational elements are further configured to determine a system reconfiguration capacity prior to utilizing the second set of configuration information to reconfigure for a second system operating mode.

29 (Currently Amended). The system of claim 28, wherein the system reconfiguration capacity is determined in a plurality of predefined units of hardware.

30 (Currently Amended). The system of claim 1, wherein the system is embodied within an integrated circuit.

31 (Currently Amended). The system of claim 1, wherein ~~a first portion of the~~ the first plurality of ~~heterogeneous~~ computational elements are operating in the first functional mode while ~~a second portion of the~~ the second plurality of ~~heterogeneous~~ computational elements are being configured for the second functional mode.

32 (Currently Amended). A method for adaptive configuration, the method comprising:

receiving a first set of configuration information, the first set of configuration information comprising a first subset of configuration information and a second subset of configuration information;

in response to the first subset of configuration information, configuring through an interconnection network a first plurality of ~~heterogeneous~~ computational elements for a first functional mode of a plurality of functional modes, ~~a first computational element of~~ the first plurality of ~~heterogeneous~~ computational elements having fixed and differing architectures; ~~a first fixed architecture and a second computational element of the plurality of heterogeneous computational elements having a second fixed architecture, the first fixed architecture being different than the second fixed architecture; and~~

in response to the second subset of configuration information, configuring ~~reconfiguring~~ through the interconnection network ~~the~~ a second plurality of ~~heterogeneous~~ computational elements for a second, different ~~second~~ functional mode of the plurality of functional modes; and ~~modes, the first functional mode being different than the second functional mode.~~

selectively routing, through the interconnection network, data and the first subset of configuration information to the first plurality of computational elements and data and the second subset of configuration information to the second plurality of heterogeneous computational elements.

33 (Original). The method of claim 32, wherein the first set of configuration information provides a first operating mode.

34 (Original). The method of claim 32, further comprising:

receiving a second set of configuration information, the second set of configuration information providing a second operating mode.

35 (Currently Amended). The method of claim 34, wherein the first set of configuration information corresponds to a first configuration ~~reconfiguration~~ capacity and the second set of configuration information corresponds to a second configuration ~~reconfiguration~~ capacity.

36 (Original). The method of claim 32, further comprising:

selecting the first set of configuration information from a plurality of sets of configuration information.

37 (Original). The method of claim 32, further comprising:

storing the first set of configuration information in a memory.

38 (Previously Presented). The method of claim 32, further comprising:

storing the first set of configuration information in a second plurality of heterogeneous computational elements configured for a memory functional mode.

39 (Previously Presented). The method of claim 32, further comprising:

storing the first set of configuration information as a configuration of the plurality of heterogeneous computational elements.

40 (Original). The method of claim 32, further comprising:

storing the first set of configuration information in a machine-readable medium.

41 (Currently Amended). The method of claim 32, wherein the first set of configuration information is received through a wireless ~~an air~~ interface.

42 (Original). The method of claim 32, wherein the first set of configuration information is received through a wireline interface.

43 (Original). The method of claim 32, wherein the first set of configuration information is embodied as a plurality of discrete information data packets.

44 (Original). The method of claim 32, wherein the first set of configuration information is embodied as a stream of information data bits.

45 (Currently Amended). The method of claim 32, wherein the first fixed architecture and the second fixed architecture are selected from a plurality of fixed ~~specific~~ architectures, the plurality of fixed ~~specific~~ architectures comprising circuitry adapted to perform at least two of the following corresponding functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability.

46 (Previously Presented). The method of claim 32, wherein the plurality of functional modes comprises at least two of the following functional modes: linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.

47 (Original). The method of claim 32, wherein the first subset of configuration information and the second subset of configuration information are commingled with data to form a singular bit stream.

48 (Original). The method of claim 32, further comprising:

directing and scheduling the configuration of the plurality of heterogeneous computational elements for the first functional mode and the reconfiguration of the plurality of heterogeneous computational elements for the second functional mode.

49 (Original). The method of claim 32, further comprising:

timing and scheduling the configuration and reconfiguration of the plurality of heterogeneous computational elements with corresponding data.

50 (Original). The method of claim 32, further comprising:

selecting the first subset of configuration information and the second subset of configuration information from a singular bit stream containing data commingled with the first set of configuration information.

51 (Original). The method of claim 32, wherein the method is operable within a mobile station having a plurality of operating modes.

52 (Previously Presented). The method of claim 51, wherein the plurality of operating modes of the mobile station comprises at least two of the following modes: a mobile telecommunication mode, a personal digital assistance mode, a multimedia reception mode, a mobile packet-based communication mode, and a paging mode.

53 (Original). The method of claim 32, wherein the method is operable within a server having a plurality of operating modes.

54 (Original). The method of claim 32, wherein the method is operable within an adjunct network entity having a plurality of operating modes.

55 (Original). The method of claim 32, further comprising:

configuring the plurality of heterogeneous computational elements to generate a request for a second set of configuration information, the second set of configuration information providing a second operating mode.

56 (Original). The method of claim 55, further comprising:

determining reconfiguration capacity prior to utilizing the second set of configuration information to reconfigure the plurality of heterogeneous computational elements for a second operating mode.

57 (Original). The method of claim 56, wherein reconfiguration capacity is determined in a plurality of predefined units of hardware.

58 (Original). The method of claim 32, wherein the method is operable within an integrated circuit.

59 (Original). The method of claim 32, further comprising:
authorizing the reception of the first set of configuration information.

60 (Original). The method of claim 32, further comprising:
requesting authorization to receive the first set of configuration information.

61 (Original). The method of claim 32, further comprising:
decrypting the first set of configuration information.

62 (Original). The method of claim 32, further comprising:
operating a first portion of the plurality of heterogeneous computational elements in the first functional mode while configuring a second portion of the plurality of heterogeneous computational elements for the second functional mode.

63 (Currently Amended). A method for adaptive configuration, the method comprising:

transmitting a first set of configuration information, the first set of configuration information comprising a first subset of configuration information and a second subset of configuration information;

wherein when the first set of configuration information is received, ~~has been received,~~ configuring through an interconnection network ~~coupled to a plurality of heterogeneous computational elements is capable of configuring the~~ a first plurality of ~~heterogeneous~~ fixed and differing computational elements for a first functional mode of a plurality of functional modes in response to the first subset of configuration information, and ~~the interconnection network further~~a second plurality of fixed and differing computational elements ~~capable of reconfiguring the plurality of heterogeneous computational elements for a second~~ for a second, different functional mode of the plurality of functional modes in response to the second subset of configuration information; and

selectively routing, through the interconnection network, data and the first subset of configuration information to the first plurality of computational elements and data and the second subset of configuration information to the second plurality of heterogeneous computational elements.

~~information, the first functional mode being different than the second functional mode; and~~

~~wherein the plurality of heterogeneous computational elements include a first computational element and a second computational element, the first computational element having a first fixed architecture and the second computational element having a second fixed architecture, the first fixed architecture being different than the second fixed architecture.~~

64 (Original). The method of claim 63, wherein the first set of configuration information, when received, provides a first operating mode.

65 (Original). The method of claim 64, further comprising:

transmitting a second set of configuration information, the second set of configuration information, when received, providing a second operating mode.

66 (Currently Amended). The method of claim 65, wherein the first set of configuration information corresponds to a first configuration ~~reconfiguration~~ capacity and the second set of configuration information corresponds to a second configuration ~~reconfiguration~~ capacity.

67 (Original). The method of claim 63, further comprising:

selecting the first set of configuration information from a plurality of sets of configuration information.

68 (Original). The method of claim 63, further comprising:

accessing the first set of configuration information in a memory.

69 (Previously Presented). The method of claim 63, further comprising:

accessing the first set of configuration information in a second plurality of heterogeneous computational elements configured for a memory functional mode.

70 (Original). The method of claim 63, further comprising:

accessing the first set of configuration information in a machine-readable medium.

71 (Currently Amended). The method of claim 63, wherein the first set of configuration information is transmitted through a wireline ~~an air~~ interface.

72 (Original). The method of claim 63, wherein the first set of configuration information is transmitted through a wireline interface.

73 (Original). The method of claim 63, wherein the first set of configuration information is embodied as a plurality of discrete information data packets.

74 (Original). The method of claim 63, wherein the first set of configuration information is embodied as a stream of information data bits.

75 (Currently Amended). The method of claim 63, wherein the first fixed architecture and the second fixed architecture are selected from a plurality of fixed ~~specific~~ architectures, the plurality of fixed ~~specific~~ architectures comprising circuitry adapted to perform at least two of the following corresponding functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability.

76 (Previously Presented). The method of claim 63, wherein the plurality of functional modes comprises at least two of the following functional modes: linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.

77 (Original). The method of claim 63, wherein the transmission step further comprises commingling data with the first subset of configuration information and the second subset of configuration information to form a singular bit stream.

78 (Original). The method of claim 63, wherein the method is operable within a wireless transmitter.

79 (Original). The method of claim 63, wherein the method is operable within a server.

80 (Original). The method of claim 63, wherein the method is operable within an adjunct network entity.

81 (Original). The method of claim 63, wherein the method is operable within an integrated circuit.

82 (Original). The method of claim 63, wherein the method is operable within a local area network.

83 (Original). The method of claim 63, wherein the method is operable within a wide area network.

84 (Original). The method of claim 63, wherein the method is operable within a wireline transmitter.

85 (Original). The method of claim 63, further comprising:

receiving a request for transmission of a second set of configuration information, the second set of configuration information providing a second operating mode.

86 (Original). The method of claim 63, further comprising:

authorizing the transmission of the first set of configuration information.

87 (Original). The method of claim 63, further comprising:

requesting an authorization to transmit the first set of configuration information.

88 (Original). The method of claim 63, further comprising:

encrypting the first set of configuration information.

89 (Currently Amended). An ~~adaptive~~ integrated circuit, comprising:

a memory adapted to store ~~a plurality of sets of~~ configuration information, the ~~plurality of sets of~~ configuration information comprising first ~~a first set of~~ configuration information and ~~a second set of~~ second configuration information;

a plurality of configurable ~~reconfigurable~~ matrices, the plurality of configurable ~~reconfigurable~~ matrices comprising a plurality of fixed and differing computational elements, ~~including a plurality of heterogeneous computation units, each heterogeneous computation unit of the plurality of heterogeneous computation units formed from a selected configuration, of a plurality of configurations, of a plurality of fixed computational elements, the plurality of fixed computational elements including a first computational element having a first architecture and a second computational element having a second architecture, the first architecture distinct from the second architecture, the plurality of heterogeneous computation units~~ the plurality of fixed and differing computational elements coupled to an interconnect network and ~~reconfigurable~~ configurable in response to the ~~plurality of sets of~~ configuration information; and

a matrix interconnection network coupled to the plurality of configurable ~~reconfigurable~~ matrices, the matrix interconnection network adapted to transfer data and configuration information to the plurality of configurable matrices. ~~capable of configuring the plurality of reconfigurable matrices in response to the first set of configuration information for a first operating mode and to reconfigure the plurality of reconfigurable matrices in response to the second set of configuration information for a second operating mode.~~

90 (Currently Amended). The ~~adaptive~~ integrated circuit of claim 89, further comprising:

a controller coupled to the plurality of reconfigurable matrices, the controller ~~capable of providing the plurality of sets of~~ adapted to direct a transfer of the configuration information from the memory to the reconfigurable matrices ~~and to the matrix interconnection network~~.

91 (Currently Amended). An ~~adaptive~~ integrated circuit, comprising:

a memory adapted to store a set of configuration information, the set of configuration information comprising a first subset of configuration information and a second subset of configuration information;

first and second pluralities of ~~a plurality of~~ heterogeneous computational elements; ~~elements, a first computational element of the plurality of heterogeneous computational elements having a first fixed architecture and a second computational element of the plurality of heterogeneous computational elements having a second fixed architecture, the first fixed architecture being different than the second fixed architecture;~~

an interconnection network coupled to the first and second pluralities ~~plurality~~ of heterogeneous computational elements, the interconnection network comprising a plurality of routing elements and a first and second pluralities of switching elements, the first plurality of switching elements ~~the interconnection network~~ capable of configuring the first plurality of heterogeneous computational elements for a first functional mode of a plurality of functional modes in response to the first subset of configuration information, **[[**and**]]** the second plurality of switching elements ~~the interconnection network further capable of reconfiguring the~~ capable of configuring the second plurality of heterogeneous computational elements for a ~~second~~ second, different functional mode of the plurality of functional modes in response to the second subset of configuration information, the routing elements capable of differentially routing data and configuration information to the first and second pluralities of heterogeneous computational elements.

~~information, the first functional mode being different than the second functional mode;~~

~~wherein a first subset of the plurality of heterogeneous computational elements is configured for a controller operating mode, the controller operating mode comprising at least one of the following functions: directing configuration and reconfiguration of the plurality of heterogeneous computational elements, selecting the first subset of configuration information and the second subset of configuration information from a singular bit stream containing data commingled with the set of configuration information, and scheduling the configuration and reconfiguration of the plurality of heterogeneous computational elements with corresponding data; and~~

~~wherein a second subset of the plurality of heterogeneous computational elements is configured for a memory operating mode for storing the set of configuration information.~~

92 (Currently Amended). The ~~adaptive~~ integrated circuit of claim 91, wherein the first subset of the plurality of heterogeneous computational elements ~~and the second subset of the plurality of heterogeneous computational elements~~ are distributed among the plurality of heterogeneous computational elements.

93 (Currently Amended). An adaptive integrated circuit, comprising:

a memory adapted to store configuration information; ~~a set of configuration information~~

a plurality of computational elements having fixed and differing circuit architectures; ~~, the set of configuration information including a first subset of configuration information and a second subset of configuration information;~~

~~a plurality of heterogeneous computational elements, a first computational element of the plurality of heterogeneous computational elements having a first fixed architecture and a second computational element of the plurality of heterogeneous computational elements having a second fixed architecture of a plurality of fixed architectures, the first fixed architecture being different than the second fixed architecture, and the plurality of fixed architectures comprising at least two of the following functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability; and~~

an interconnection network coupled to the plurality of ~~heterogeneous~~ computational elements, the interconnection network comprising a plurality of routing elements and a plurality of switching elements, the interconnection network capable of configuring the plurality of ~~heterogeneous~~ computational elements for ~~a first functional mode of~~ a plurality of functional modes in response to the configuration information by selectively routing data to the plurality of computational elements and selectively switching input and output connections between selected computational elements of the plurality of computational elements. ~~in response to the first subset of configuration information, and the interconnection network further capable of reconfiguring the plurality of heterogeneous computational elements for a second functional mode of the plurality of functional modes in response to the second subset of configuration information~~

~~, the first functional mode being different than the second functional mode, and the plurality of functional modes comprising at least two of the following functional modes: linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.~~

94 (Currently Amended). An ~~adaptive~~ integrated circuit, comprising:

~~configuration information;~~

a first plurality of fixed and differing computational elements; and

an interconnection network coupled to the first plurality of ~~fixed and differing~~ computational elements, the interconnection network comprising a plurality of routing elements, the interconnection network adapted to configure ~~capable of responding to the configuration information to configure and reconfigure the~~ the first plurality of ~~fixed and differing~~ computational elements for a first functional mode of a plurality of functional modes in response to first configuration information.

95 (Currently Amended). The ~~adaptive~~ integrated circuit of claim 94, wherein the first configuration information provides an operating mode.

96 (Currently Amended). The ~~adaptive~~ integrated circuit of claim 94, wherein the plurality of functional modes comprises at least two of the following functional modes: linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.

97 (Currently Amended). The ~~adaptive~~ integrated circuit of claim 94, wherein the first configuration information is stored in at least one computational element, ~~a portion~~ of the first plurality of ~~fixed and differing~~ computational elements, ~~elements~~ configured for a memory functional mode.

98 (Currently Amended). The ~~adaptive~~ integrated circuit of claim 94, wherein the first configuration information is stored as a configuration of the first plurality of ~~fixed and differing~~ computational elements.

99 (Currently Amended). The ~~adaptive~~ integrated circuit of claim 94, wherein the first plurality of ~~fixed and differing~~ computational elements are selected from a plurality of ~~specific~~ fixed circuitry architectures, the plurality of fixed circuitry ~~specific~~ architectures comprising circuitry adapted to perform at least two of the following functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability.

100 (Currently Amended). The ~~adaptive~~ integrated circuit of claim 94, wherein the first plurality of ~~fixed and differing~~ computational elements are configured to identify and select the first configuration information from a singular bit stream containing data commingled with the first configuration information.

101 (New). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network, the second plurality of computational elements comprising at least one computational element which is different than the computational elements comprising the first plurality of computational elements.

102 (New). The integrated circuit of claim 101, wherein the interconnection network is further adapted to independently configure the first plurality of computational elements in response to the first configuration information and configure the second plurality of computational elements in response to second configuration information.

103 (New). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the interconnection network is further adapted to configure the first plurality of computational elements and the second plurality of computational elements by selectively routing data to the first plurality of computational elements and the second plurality of computational elements.

104 (New). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the interconnection network further comprises a plurality of switching elements, and wherein the interconnection network is further adapted to configure the first plurality of computational elements and the second plurality of computational elements by selectively switching data to the first plurality of computational elements and the second plurality of computational elements.

105 (New). The integrated circuit of claim 104, wherein the second plurality of computational elements further comprises at least one computational element which is different than the computational elements comprising the first plurality of computational elements.

106 (New). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the interconnection network further comprises a plurality of switching elements, and wherein the interconnection network is further adapted to configure the first plurality of computational elements and the second plurality of computational elements by selectively switching or routing data to the first plurality of computational elements and the second plurality of computational elements.

107 (New). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the interconnection network is further adapted to configure the second plurality of computational elements in response to second configuration information; and

wherein the interconnection network is further adapted to additionally configure both the first plurality of computational elements and the second plurality of computational elements for a third functional mode of the plurality of functional modes by selectively routing data to the first plurality of computational elements and the second plurality of computational elements.

108 (New). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the interconnection network is further adapted to configure the second plurality of computational elements in response to second configuration information; and

wherein the interconnection network is further adapted to additionally configure both the first plurality of computational elements and the second plurality of computational elements for a third functional mode of the plurality of functional modes by selectively switching data to the first plurality of computational elements and the second plurality of computational elements.

109 (New). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the interconnection network is further adapted to configure the second plurality of computational elements in response to second configuration information; and

wherein the interconnection network is further adapted to selectively route data and the first subset of configuration information to the first plurality of computational elements and route data and the second subset of configuration information to the second plurality of computational elements.

110 (New). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the plurality of routing elements are adapted for self-routing of data packets to the first and second pluralities of computational elements.

111 (New). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the plurality of routing elements are adapted for self-routing of first configuration information to the first plurality of computational elements and self-routing of second configuration information to the second plurality of computational elements.

112 (New). The integrated circuit of claim 94, further comprising:

a memory coupled to the interconnection network, the memory adapted to store the first configuration information.

113 (New). The integrated circuit of claim 94, wherein the interconnection network further comprises a plurality of switching elements and a data interface circuit, and wherein the interconnection network is further adapted to configure the first plurality of computational elements by selectively routing data through the data interface circuit for transfer to the first plurality of computational elements and selectively switching data input and output connections between the computational elements comprising the first plurality of computational elements.

114 (New). The integrated circuit of claim 94, further comprising:

a data interface circuit coupled to the first plurality of computational elements and to the interconnection network;

wherein the interconnection network further comprises a plurality of switching elements, wherein the plurality of routing elements of the interconnection network are adapted to selectively route data to the data interface circuit for transfer to the first plurality of computational elements, and wherein the plurality of switching elements of the interconnection network are adapted to configure the first plurality of computational elements by selectively switching data input and output connections between the computational elements comprising the first plurality of computational elements.

115 (New). The system of claim 1, wherein the second plurality of computational elements further comprises at least one computational element which is different than the computational elements comprising the first plurality of computational elements.

116 (New). The system of claim 1, wherein the interconnection network is further adapted to independently configure the first plurality of computational elements and the second plurality of computational elements.

117 (New). The system of claim 1, wherein the interconnection network is further adapted to configure the first plurality of computational elements and the second plurality of computational elements by selectively routing data to the first plurality of computational elements and the second plurality of computational elements.

118 (New). The system of claim 1, wherein the interconnection network is further adapted to configure the first plurality of computational elements and the second plurality of computational elements by selectively switching data to the first plurality of computational elements and the second plurality of computational elements.

119 (New). The system of claim 1, wherein the second plurality of computational elements further comprises at least one computational element which is different than the computational elements comprising the first plurality of computational elements, and wherein the interconnection network is further adapted to configure the first plurality of computational elements and the second plurality of computational elements by selectively switching data to the first plurality of computational elements and the second plurality of computational elements.

120 (New). The system of claim 1, wherein the interconnection network is further adapted to additionally configure both the first plurality of computational elements and the second plurality of computational elements for a third functional mode of the plurality of functional modes by selectively routing data to the first plurality of computational elements and the second plurality of computational elements.

121 (New). The system of claim 1, wherein the interconnection network is further adapted to additionally configure both the first plurality of computational elements and the second plurality of computational elements for a third functional mode of the plurality of functional modes by selectively switching data to the first plurality of computational elements and the second plurality of computational elements.

122 (New). The system of claim 1, wherein the interconnection network is further adapted to selectively route data and the first subset of configuration information to the first plurality of computational elements and route data and the second subset of configuration information to the second plurality of computational elements.

123 (New). The system of claim 1, wherein the plurality of routing elements are adapted for self-routing of data packets to the first and second pluralities of computational elements.

124 (New). The system of claim 1, wherein the plurality of routing elements are adapted for self-routing of the first subset of configuration information to the first plurality of computational elements and self-routing of the second subset of configuration information to the second plurality of computational elements.

125 (New). The system of claim 1, wherein the interconnection network further comprises a first data interface circuit coupled to the first plurality of computational elements and a second data interface circuit coupled to the second plurality of computational elements, wherein the interconnection network is further adapted to configure the first plurality of computational elements by selectively routing data through the first data interface circuit for transfer to the first plurality of computational elements and selectively switching data input and output connections between the computational elements comprising the first plurality of computational elements, and wherein the interconnection network is further adapted to configure the second plurality of computational elements by selectively routing data through the second data interface circuit for transfer to the second plurality of computational elements and selectively switching data input and output connections between the computational elements comprising the second plurality of computational elements.

126 (New). The system of claim 1, further comprising:

a first data interface circuit coupled to the first plurality of computational elements and to the interconnection network;

a second data interface circuit coupled to the second plurality of computational elements and to the interconnection network;

wherein the plurality of routing elements of the interconnection network are adapted to route data selectively to the first data interface circuit for transfer to the first plurality of computational elements and to the second data interface circuit for transfer to the second plurality of computational elements, wherein the plurality of switching elements of the interconnection network are adapted to configure the first plurality of computational elements by selectively switching data input and output connections between the computational elements comprising the first plurality of computational elements, and wherein the plurality of switching elements of the interconnection network are adapted to configure the second plurality of computational elements by selectively switching data input and output connections between the computational elements comprising the second plurality of computational elements.

127 (New). The system of claim 1, wherein the plurality of switching elements comprise a plurality of multiplexers.

128 (New). The system of claim 1, wherein the plurality of switching elements comprise a plurality of demultiplexers.

129 (New). An integrated circuit, comprising:

a first plurality of fixed and differing computational elements forming a first configurable architecture;

an interconnection network coupled to the first plurality of computational elements, the interconnection network adapted to transfer data and first configuration information to the first plurality of computational elements.

130 (New). The integrated circuit of claim 129, wherein the interconnection network comprises a plurality of routing elements and a plurality of switching elements.

131 (New). The integrated circuit of claim 130, further comprising:

a second plurality of fixed and differing computational elements forming a second, different configurable architecture;

wherein the interconnection network is further adapted to transfer data and second configuration information to the first plurality of computational elements.

132 (New). The integrated circuit of claim 131, wherein the interconnection network is further adapted to configure the first plurality of computational elements for a first functional mode of a plurality of functional modes in response to the first configuration information and to independently configure the second plurality of computational elements for a second functional mode of the plurality of functional modes in response to the second configuration information.

133 (New). The integrated circuit of claim 132, wherein the interconnection network is further adapted to configure the first plurality of computational elements and the second plurality of computational elements by selectively routing or selectively switching data to the first plurality of computational elements and the second plurality of computational elements.

134 (New). The integrated circuit of claim 132, wherein the interconnection network is further adapted to additionally configure both the first plurality of computational elements and the second plurality of computational elements for a third functional mode of the plurality of functional modes by selectively routing or switching data to the first plurality of computational elements and the second plurality of computational elements.

135 (New). The integrated circuit of claim 130, wherein the plurality of routing elements are adapted for self-routing of data packets to the first plurality of computational elements.

136 (New). The integrated circuit of claim 130, wherein the plurality of routing elements are adapted for self-routing of first configuration information to the first plurality of computational elements.

137 (New). The integrated circuit of claim 130, wherein the interconnection network further comprises a data interface circuit, and wherein the interconnection network is further adapted to configure the first plurality of computational elements by selectively routing data through the data interface circuit for transfer to the first plurality of computational elements and selectively switching data input and output connections between the computational elements comprising the first plurality of computational elements.

138 (New). The integrated circuit of claim 130, further comprising:

a data interface circuit coupled to the first plurality of computational elements and to the interconnection network;

wherein the plurality of routing elements of the interconnection network are adapted to selectively route data to the data interface circuit for transfer to the first plurality of computational elements, and wherein the plurality of switching elements of the interconnection network are adapted to configure the first plurality of computational elements by selectively switching data input and output connections between the computational elements comprising the first plurality of computational elements.

139 (New). An integrated circuit, comprising:

a first plurality of fixed and differing computational elements forming a first reconfigurable circuit;

a second plurality of fixed and differing computational elements forming a second, different configurable circuit; and

an interconnection network coupled to the first and second pluralities of computational elements, the interconnection network comprising a plurality of routing elements and a plurality of switching elements, the interconnection network adapted to configure the first plurality of computational elements for a first functional mode of a plurality of functional modes in response to first configuration information and to independently configure the second plurality of computational elements in response to second configuration information by selectively routing or switching data to the first plurality of computational elements and the second plurality of computational elements.

140 (New). The integrated circuit of claim 139, wherein the interconnection network is further adapted to selectively route data and the first configuration information to the first plurality of computational elements and route data and the second configuration information to the second plurality of computational elements.

141 (New). The integrated circuit of claim 139, wherein the plurality of routing elements are adapted for self-routing of data packets to the first and second pluralities of computational elements.

142 (New). The integrated circuit of claim 139, wherein the plurality of routing elements are adapted for self-routing of first configuration information to the first plurality of computational elements and self-routing of second configuration information to the second plurality of computational elements.

143 (New). The integrated circuit of claim 139, further comprising:

a first data interface circuit coupled to the first plurality of computational elements and to the interconnection network;

a second data interface circuit coupled to the second plurality of computational elements and to the interconnection network;

wherein the plurality of routing elements are adapted to selectively route data to the first data interface circuit for transfer to the first plurality of computational elements and to selectively route data to the second data interface circuit for transfer to the second plurality of computational elements, and wherein the plurality of switching elements are adapted to configure the first plurality of computational elements by selectively switching data input and output connections between the computational elements comprising the first plurality of computational elements and to configure the second plurality of computational elements by selectively switching data input and output connections between the computational elements comprising the second plurality of computational elements.